# Kevin Rahsaz

*Software Engineer | High-Performance Computing & Signal Processing*

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## Summary

Software Engineer with a relentless focus on high-performance computing and applied mathematics. Proven experience architecting C++/Python hybrid frameworks for real-time signal processing, bridging the gap between theoretical modeling and production-grade infrastructure. Thrives in ambiguous environments requiring end-to-end ownership, from initial experimentation to shipping optimized results. Seeking to apply expertise in numerical analysis, simulation, and systems engineering to build mission-critical infrastructure, distributed systems, and data-intensive computing platforms.

## Education

Feb 2022 – May 2026 **Bachelor of Science in Computer Science**, *University of Phoenix*, Phoenix, AZ

- **GPA:** 3.83/4.00
- **Relevant Coursework:** Algorithmic Theory and Practice, Software Architecture, Calculus I & II, Linear Algebra, Discrete Math, Computer Organization and Architecture, Intro to Operating Systems.

## Technical Skills

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| **Languages** | C++ (17), Python 3, CUDA C/C++, Bash, PowerShell |
| **Core** | CMake, MSVC, Docker, Git, PyBind11, GitHub Actions, Hydra, Pydantic, Snakemake, MLFlow, Streamlit |
| **Concepts** | Heterogeneous Computing (CPU/GPU), Real-time Systems, Multithreading, Lock-free/Thread-Safe Structures, Signal Processing (FFT, STFT), Zero-Copy, Latency Hiding, IEEE 754 |
| **Tools** | NVIDIA GPUs (cuFFT, Nsight), Linux (Ubuntu), Windows 11 |

## Experience

Feb 2025 – Feb 2026 **Research Software Engineer (Volunteer)**, *Sensor's Energy and Automation Laboratory (SEAL)*, University of Washington, Seattle, WA

- **Lead Architect (SigTekX):** Spearheaded the design and integration of a hybrid Python/C++ framework for processing high-bandwidth RF data, driving technical strategy from inception to artifact build.
- **High-Performance Architecture:** Designed and implemented a **zero-copy, thread-safe ring buffer** in C++17 to decouple acquisition from processing, ensuring deterministic latency for hardware integration.
- **GPU Acceleration:** Implemented **CUDA-accelerated pipelines** using NVIDIA **cuFFT** to offload heavy spectral analysis (STFT), verifying correctness against CPU reference implementations.
- **Optimization & Stability:** Engineered a **GPU clock locking** mechanism to prevent thermal throttling during benchmarks. Enforced **IEEE 754-2019** compliance using FMA operations for precision.
- **Validation Strategy:** Structured validation using **IEEE 829-2008** standards. Designed robust **Pydantic** schemas to enforce strict type safety for complex signal parameters, preventing runtime failures.
- **Performance Dashboard:** Developed an interactive **Streamlit** tool to visualize offline benchmarks and automate accuracy verification plots (C++ vs. NumPy reference models).
- **Infrastructure & CI/CD:** Implemented a GitHub Actions pipeline for build verification and code formatting (Clang-Format). Containerized development with **Docker** to standardize CUDA dependencies.
- **Reproducible Research:** Orchestrated workflows with **Snakemake** and **Hydra**, automating parameter sweeps (Optuna) and static figure generation for performance reports.
- **Cross-Platform:** Managed lifecycle for **Windows 11 (MSVC)** and **Linux (Ubuntu)**, configuring packaging (pyproject.toml) to build installable wheels for PyPI.
- **Systems Engineering:** Produced technical feasibility documentation for the 'Ionosense' ULF/VLF antenna system, analyzing **2024 Perseid meteor shower** data to support grant applications for **NASA**, **US Space Force**, and the **NSF**.